tems at microwave frequencies rather than impedance data. Further, a wave approach to the problem enables more complicated oscillator structures to be investigated through the relatively easy application of Mason's topological rules to the flowgraph description.

From the investigation of a mildly nonlinear device/circuit interaction such that noise modulations pass linearly around the oscillator we have derived formulas for oscillation condition and stability. Expressions for the amplitude and phase noise of the oscillator have also been derived. A graphical interpretation of these conditions has been presented in terms of the circuit reflection coefficient and inverse device reflection coefficient loci in a cylindrical coordinate system. The results of this graphical investigation have been shown to be equivalent to those derived by Kurokawa.

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# RF Characterization of Microwave Power FET's

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*Abstract*— **The large-signal $S$-parameter $S_{22}$ and the optimum load for maximum output power are two parameters commonly used in the RF characterization of microwave power FET's. Using a nonlinear circuit model of the device, the dependence on RF power of each of these parameters is investigated. A method is given for computing the optimum load from the large-signal $S_{22}$. Equivalent load-pull data can thus be obtained without the need for load-pull measurements. The gain compression characteristics of the transistor for arbitrary load can be computed from large-signal $S_{21}$ and $S_{22}$ data.**

## I. Introduction

IN THE ANALYSIS and design of GaAs FET power amplifiers there is a need for data on device RF characteristics at large-signal levels. Experimental methods for obtaining these data fall into two main classes: large-signal $S$-parameter measurements [1], [2] and load-pull measurements [3]–[7]. Large-signal $S$-parameters are an extension of the well-known small-signal $S$-parameters [8] and are generally measured with fixed 50-Ω terminations at the device terminals. Load-pull measurements differ from large-signal $S$-parameter measurements in that the terminations are not held constant. The device is driven at a given input power level and parameters such as output power [3] or intermodulation distortion [7] are measured as a function of the load admittance. A load-pull parameter which is particularly useful in the design of power-amplifiers is the *optimum load admittance for maximum output power* [3], [4].

The variable load admittance used in load-pull measurements can be set up either using a tuner [3], [6] or with a second signal injected at the output port of the device [4], [5], [7]. Both of these loading techniques give circuit conditions which closely resemble those the FET will experience in an amplifier. Therefore, the main advantage of load-pull data over large-signal $S$-parameter data is that they are measured under realistic operating conditions. As a result, load-pull data are well suited to analysis and design procedures.

Large-signal $S$-parameter measurements are generally easier and less tedious to implement than load-pull measurements. In addition, large-signal $S$-parameters can be readily measured on a swept-frequency basis. Unfortunately, large-signal $S$-parameters are less useful than load-pull data in circuit analysis and design. This problem arises because small-signal $S$-parameters (and thus large-signal $S$-parameters) are defined in terms of a *linear* two-port network [8]. Under large-signal conditions, a microwave transistor is nonlinear and large-signal $S$-parameters cannot be used to predict the large-signal device performance for terminations other than the fixed terminations used during measurement. In addition, it is not clear what signal power level should be used for large-signal $S$-parameter measurements.

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To explain the behavior of large-signal $S$-parameters and to determine their relationship to load-pull parameters, it is necessary to carry out a nonlinear circuit analysis of the FET. Nonlinear circuit models have been used previously in the analysis of FET circuits to determine intermodulation distortion [9], [10], gain compression, [9], [11], [12], and optimum load admittance for maximum output power [9], [11], [12]. However, these characteristics have not been compared with the large-signal $S$-parameters.

The present paper describes an approximate analysis of large-signal FET characteristics. The analysis is based on a simplified nonlinear unilateral circuit model of the device. Expressions are obtained for the large-signal output conductance and for the load conductance for maximum output power. It is shown that at large-signal levels these two conductances are different. A method is given which enables the optimum load conductance to be calculated from measured large-signal $S_{22}$ data. Thus equivalent load-pull data can be obtained from large-signal $S$-parameters without the need for load-pull measurements.

## II. Experimental Large-Signal Data

As an illustration of large-signal $S$-parameters and optimum load characteristics, Fig. 1 shows measured data for a common-source connected 550-$\mu$m gate-width GaAs FET.[1] The device chip was mounted in a 50-$\Omega$ microstrip package and was wire-bonded to the 50-$\Omega$ microstrip input and output lines. All measurements were referenced to the device contact pads and reflection coefficients were determined with a manual network analyzer. The optimum load was measured using a 50-$\Omega$ source impedance at the gate and a coaxial slug tuner as a variable load at the drain. The measurement frequency was 6 GHz and the device was biased to a drain voltage of $V_{DS}=7$ V and a gate voltage of $V_{GS}=-0.8$ V. This gate bias was selected such that for an incident or available input power level of 19.3 dBm the output power (23 dBm) was maximized. The associated gain compression ratio was 2.9 dB. With zero RF input power, the drain current at the gate bias of $-0.8$ V was approximately $I_{DSS}/2$.

The large-signal $S$-parameters were measured with the incident RF power level (in dBm) as a parameter. For $S_{11}$ and $S_{21}$ the incident power $P_{a1}$ at the input port was varied from a value of 0 dBm (approximately small signal) up to a maximum of 20 dBm. For $S_{22}$ and $S_{12}$ the incident power $P_{a2}$ at the output port was varied from 0 to 29 dBm. This maximum $P_{a2}$ is considerably larger than the nominal 23-dBm output power capability of the device. Reasons for using such a high incident power level are given later.

It is clear from Fig. 1 that all four of the large-signal $S$-parameters depend on RF power level. Of particular interest here is $S_{21}$, which decreases in magnitude with increasing power level, and $S_{22}$, which approximately follows a constant susceptance line on the Smith chart. As the incident power $P_{a2}$ is increased, the large-signal output conductance increases. The measured optimum load reflection coefficient for maximum output power $\Gamma_{opt}$ in Fig. 1 is given with output power as a parameter. With increasing output power, $\Gamma_{opt}$ also approximately follows a constant susceptance line. Like the large-signal output conductance, the optimum load conductance also increases with power level. In the following section the power level dependence of each of these parameters is investigated.

[1]The devices were supplied by G. Roberts of Hewlett-Packard, Santa Rosa, CA.

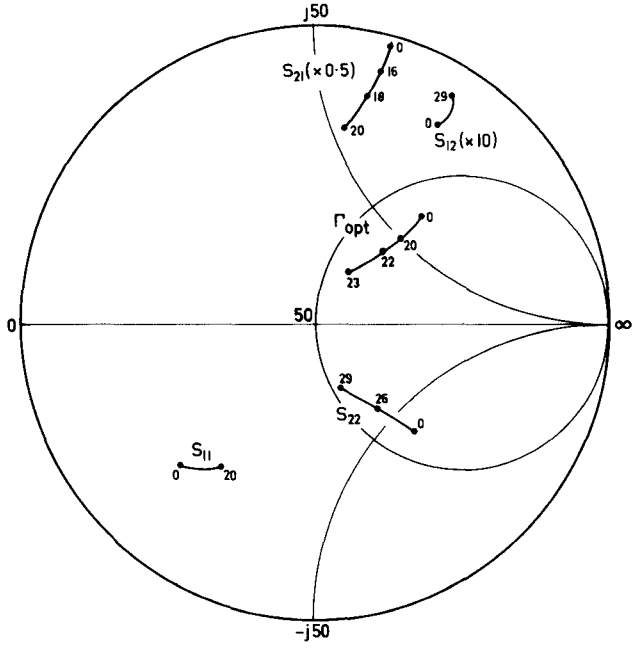


Fig. 1. Large-signal $S$-parameters and optimum load reflection coefficient $\Gamma_{opt}$ at 6 GHz for 550-$\mu$m gate-width device. The RF power level is given in dBm.

## III. Analysis

### A. Circuit Model

Fig. 2 shows the nonlinear unilateral circuit model of the FET. The device is fed from a linear source admittance $Y_s$ and is terminated with a linear load admittance $Y_L=G_L+jB_L$. The model is similar to one used previously [9] in the analysis of intermodulation distortion and gain compression. Nonlinearities in the device are lumped into two circuit elements: a nonlinear transconductance and a nonlinear output conductance. Since the output nonlinearity is usually dominant in FET power amplifiers [12], [13], the analysis presented here concentrates on the output characteristics of the device. It is assumed that the input capacitance $C_g$ is linear. Parasitic inductance in the source lead is neglected.

The nonlinear transconductance $G_m$ and the nonlinear output conductance $G_d$ are described by truncated power series expansions [9]

$$i_1=\sum_{l=1}^{3} g_{ml}v_i^l(t-\tau_l) \tag{1}$$

$$i_2=\sum_{l=1}^{3} g_l v_o^l(t) \tag{2}$$

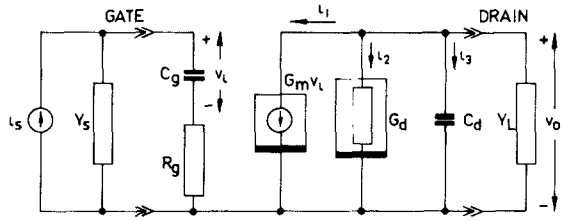


Fig. 2. Nonlinear unilateral circuit model of the transistor.

where $g_{ml}$ and $g_l$ are real expansion coefficients, $\tau_l$ are time delays, and $i_1$, $i_2$, $v_i$, and $v_o$ represent signal components of current and voltage about a fixed bias point.

It has been shown experimentally in [9] that for small to moderate gain compression ratios (up to about 2 dB) third-order intermodulation distortion in the transistor is mainly caused by third-order terms in (1) and (2). Similar experiments have been used here to determine the effect on output power of the load at the second harmonic of the carrier frequency. The optimum load measurements were repeated with an adjustable-length line, a low-pass filter, and a number of different attenuators cascaded with the tuner. With this arrangement, it was possible to adjust the second-harmonic load admittance over a wide range while keeping the carrier-frequency load fixed. It was found that, to within an experimental uncertainty of $\pm 0.2$ dB, the output power was independent of the harmonic load for output power levels up to 23 dBm. It follows that if the gain compression ratio is less than about 2–3 dB, second-harmonic signal components appearing at the output port of the transistor have little effect on the compression characteristics and can be neglected in approximate gain compression calculations. Thus it is assumed in the present analysis that $g_{m2}=g_2=0$. This approximation limits the ultimate accuracy of the analysis, but leads to simple analytical solutions.

### B. Large-Signal S-Parameters

Large-signal $S$-parameters are represented here by an upper case $S$ and small-signal $S$-parameters are represented by a lower case $s$. Since the device is assumed unilateral ($s_{12}=S_{12}=0$) and the gate circuit is assumed linear, the input reflection coefficient $S_{11}$ is constant and independent of power level. The objective in this section is to obtain expressions for $S_{21}$ and $S_{22}$.

*1) $S_{21}$:* The large-signal $S$-parameter $S_{21}$ is proportional to the voltage gain compression ratio of the FET with 50-Ω terminations. In [9], an expression is given for gain compression in terms of the device terminations and the input power level. The circuit model of the FET in [9] includes a nonlinear output capacitance. With this capacitance assumed linear in the present analysis, the voltage gain compression ratio $k$ becomes [9]

$$k=k_t k_o \tag{3}$$

where $k_t$ is the contribution of the nonlinear transconductance to the total gain compression ratio and $k_o$ is the contribution of the nonlinear output conductance. The contributions to gain compression are given by

$$k_t=1+P_{\text{in}}\beta \tag{4}$$

and

$$k_o=\left(1+P_{\text{in}}\delta|k|^2|Z|^2Z\right)^{-1} \tag{5}$$

where

$$Z=(Y_L+y_1)^{-1} \tag{6}$$

$y_1=g_1+j\omega C_d$ is the small-signal output admittance of the FET, $\omega$ is the radian frequency of the input signal, and $P_{\text{in}}$ is the input power.[2] The two device parameters $\beta$ and $\delta$ are related to nonlinearities in the transconductance and the output conductance, respectively. They are given by

$$\beta=6G_{pm}g_1g_{l1}g_{l3}\underline{/(\tau_1-\tau_3)} \tag{7}$$

and

$$\delta=6G_{pm}g_1g_3 \tag{8}$$

where $G_{pm}$ is the maximum small-signal gain.

Since $S_{21}$ is proportional to the voltage gain compression ratio, it can be written in the form

$$S_{21}=k_s s_{21} \tag{9}$$

where $k_s$ is the voltage gain compression ratio for $Y_L$ equal to $Y_0$, the characteristic admittance of the $S$-parameter test set. The gain compression ratio $k_s$ depends strongly on $P_{\text{in}}$ and $Y_0$ and it follows that $S_{21}$ is also a strong function of these parameters. In the limit as $P_{\text{in}}$ approaches zero, $k_s$ approaches unity and $S_{21}$ approaches $s_{21}$ as expected.

*2) $S_{22}$:* In the measurement of $S_{22}$, a signal is applied at the output port of the device from a generator of internal admittance $Y_0$. Since no signal is applied at the input port, the transconductance current $i_1$ (Fig. 2) is zero. The large-signal $S_{22}$ is given by

$$S_{22}=\frac{Y_0-Y_{\text{out}}}{Y_0+Y_{\text{out}}} \tag{10}$$

where $Y_{\text{out}}=G_{\text{out}}+jB_{\text{out}}$ is the large-signal output admittance. This output admittance is given by

$$Y_{\text{out}}=\frac{I_2+I_3}{V_o} \tag{11}$$

where $I_2$, $I_3$, and $V_o$ are phasor quantities. From [9] it is easily shown that

$$I_2+I_3=V_o\left(y_1+\frac{3}{4}g_3|V_o|^2\right). \tag{12}$$

Substituting (12) in (11), one obtains $Y_{\text{out}}$ in terms of the output voltage $V_o$

$$Y_{\text{out}}=y_1+\frac{3}{4}g_3|V_o|^2. \tag{13}$$

Note that $Y_{\text{out}}$ is independent of the generator admittance $Y_0$, but depends on $|V_o|$. At small-signal levels, where $|V_o|$

[2] In the theory sections of [9], expressions for device distortion are given in terms of *peak* power. All power quantities in the present paper are *average* values.

is small, the large-signal output admittance approaches the small-signal output admittance $y_1$. As $|V_o|$ is increased, the output conductance $G_{out}$ becomes larger than $g_1$.

It is useful to express $G_{out}$ in terms of RF power level rather than in terms of the output voltage $V_o$. In measurements of $S_{22}$, one usually monitors the available power $P_{a2}$ incident on the output port of the device. However, it is more appropriate in the present analysis to use the RF power dissipated in the device $P_d$. A normalized power level is defined here in terms of $P_d$, enabling a simple relationship to be obtained between the power level and the normalized large-signal output conductance $g_{out} = G_{out}/g_1$. The normalized power level $P_{ns}$ is given by

$$P_{ns} = \frac{P_d g_3}{g_1^2} = \frac{P_d \delta}{6 g_1^2 G_{pm}} \tag{14}$$

where

$$P_d = \frac{|V_o|^2 G_{out}}{2}. \tag{15}$$

Substituting (14) and (15) in (13), one obtains

$$\left.\begin{aligned} P_{ns} &= \frac{2}{3}\left(g_{out}^2 - g_{out}\right), \qquad g_{out} \geq 1 \\ B_{out} &= j\omega C_d. \end{aligned}\right\} \tag{16}$$

*C. Optimum Load Admittance*

The optimum load admittance is measured with a constant RF signal level applied at the input port of the device. Under these conditions, the output power is given by

$$P_{out} = P_{in} G_p |k|^2 \tag{17}$$

where $G_p$ is the small-signal power gain and $|k|^2$ is the power gain compression ratio. The small-signal power gain is given by

$$G_p = 4 G_{pm} g_1 G_L |Z|^2. \tag{18}$$

For a unilateral device, the maximum small-signal power gain $G_{pm}$ is equal to the maximum small-signal available gain (MAG) [8]

$$G_{pm} = \frac{|s_{21}|^2}{\left[1-|s_{11}|^2\right]\cdot\left[1-|s_{22}|^2\right]}. \tag{19}$$

To determine the optimum load for maximum output power, the input power $P_{in}$ is assumed to be constant and (17) is differentiated with respect to $Y_L$. The derivative is set to zero, yielding

$$G_p \frac{\partial |k|^2}{\partial G_L} + |k|^2 \frac{\partial G_p}{\partial G_L} = 0 \tag{20}$$

and

$$G_p \frac{\partial |k|^2}{\partial B_L} + |k|^2 \frac{\partial G_p}{\partial B_L} = 0. \tag{21}$$

The value of $Y_L$ which satisfies (20) and (21) is the *optimum load admittance for maximum output power* $Y_{opt} = G_{opt} + jB_{opt}$. The corresponding output power is $P_{out} = P_{opt}$.

The partial derivatives in (20) and (21) are evaluated using (3) and (18). Differentiation of (3) is awkward since the derivative contains terms both in $\delta$ and $\delta^2$. However, terms in $\delta^2$ are much smaller than terms in $\delta$ and are, therefore, neglected. With this simplification and after some manipulation, (20) and (21) yield

$$\left.\begin{aligned} P_{no} &= \frac{g_{opt}\left(g_{opt}^2 - 1\right)}{3\left(2 + g_{opt}\right)}, \qquad g_{opt} \geq 1 \\ B_{opt} &= -j\omega C_d \end{aligned}\right\} \tag{22}$$

where $g_{opt} = G_{opt}/g_1$ is the normalized optimum load conductance and $P_{no}$ is the normalized optimum output power level, given by

$$P_{no} = \frac{P_{opt} g_3}{g_1^2} = \frac{P_{opt}\,\delta}{6 g_1^3 G_{pm}}. \tag{23}$$

Note that the optimum load conductance $g_{opt}$ in (22) depends on the device parameter $\delta$ but is independent of $\beta$. Thus the condition for optimum load does not depend on gain compression in the nonlinear transconductance. However, if gain compression in the transconductance is large, the output power may saturate, thus limiting the maximum $P_{opt}$ obtainable from the device.

## IV. Comparison of $Y_{out}$ and $Y_{opt}$

The optimum load admittance $Y_{opt}$ can be compared with the large-signal output admittance $Y_{out}$ (and thus the large-signal $S_{22}$) using the expressions given in the previous section. Consider first the limiting case at small-signal levels. Under these conditions $P_{ns}$ and $P_{no}$ approach zero, and (16) and (22) yield $g_{out} = g_{opt} = 1$. Thus

$$Y_{opt} = Y_{out}^* \tag{24}$$

as is well known from linear circuit theory. At large-signal levels, where nonlinear effects at the output of the transistor become significant, both $G_{out}$ and $G_{opt}$ depend on power level and (24) no longer holds. This is illustrated in Fig. 3, which shows the theoretical $g_{out}$ and $g_{opt}$ plotted against the normalized power levels $P_{ns}$ and $P_{no}$ [14]. It can be seen that $g_{out}$ is different from $g_{opt}$ at comparable power levels. At $P_{no} = P_{ns} = 0.5$, for example, $g_{opt}$ is 33 percent larger than $g_{out}$. This normalized power level corresponds to a gain compression ratio of $k_o \simeq -1.0$ dB at the output.

The theoretical results shown in Fig. 3 highlight the magnitude of the errors which result if the complex conjugate of the large-signal $Y_{out}$ or $S_{22}$ is used as a measure of the optimum load. In general, large-signal $S_{22}$ measurements give estimates of load conductance which are too small. One way to reduce this discrepancy is to measure $S_{22}$ at an increased power level. This ensures that the signal voltage level at the drain is increased to a more realistic value. Fig. 3 shows that for $g_{opt} \simeq g_{out}$, the power dissipated in the device $P_d$ during the $S_{22}$ measurement should be about 6 dB greater than the optimum output power $P_{opt}$. This technique has the disadvantage that inconveniently

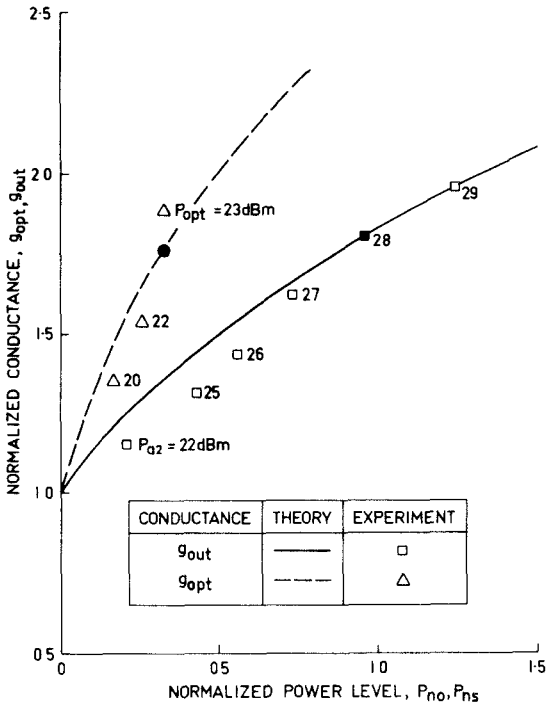


Fig. 3. Theoretical and experimental normalized conductances $g_{out}$ and $g_{opt}$ against normalized power levels $P_{no}$ and $P_{ns}$.

large power levels may be required. For example, a transistor with an output power of $P_{opt}=1$ W would require approximately 4 W of dissipated RF power. If the device were not matched to the $S$-parameter test set ($S_{22}\neq 0$), the incident power $P_{a2}$ at the output port would need to be even greater than 4 W. Thus a 1-W transistor with $|S_{22}|=0.8$ would need an incident power level of approximately 11 W.

## V. Examples

### A. $Y_{out}$ and $Y_{opt}$

The optimum load $Y_{opt}$ at a given power level can be determined from measured values of small-signal $s_{22}$ and large-signal $S_{22}$ using either (16) and (22) or the curves in Fig. 3. This has been done using the measured $S$-parameter data given in Fig. 1. The starting point for the calculation was the measured value of $S_{22}$ at a power level of $P_{a2}=28$ dBm. Normalizing the output conductance to its small-signal value (obtained from $s_{22}$), one obtains $g_{out}=1.8$ at this power level. From (16) and (14), and using the relationship

$$P_d = P_{a2}\left(1-|S_{22}|^2\right) \tag{25}$$

the coefficient $g_3$ was found to be $1.04\times 10^{-4}$ $S^2\cdot W^{-1}$. With this value of $g_3$ in (23), (22) yields $g_{opt}=1.76$ at an output power level of $P_{opt}=23$ dBm. Values of $g_{opt}$ at other power levels can easily be obtained from (22).

For comparison with the above calculated value of $g_{opt}$, the measured value at $P_{out}=23$ dBm was 1.88. Fig. 3 shows the experimentally determined $g_{out}$ and $g_{opt}$ for a range of power levels. The measured value of $g_{out}$ used to evaluate $g_3$ is indicated with a solid square and the calculated $g_{opt}$ for $P_{opt}=23$ dBm is indicated with a solid circle. The measured data show reasonable agreement with the theoretical curves.

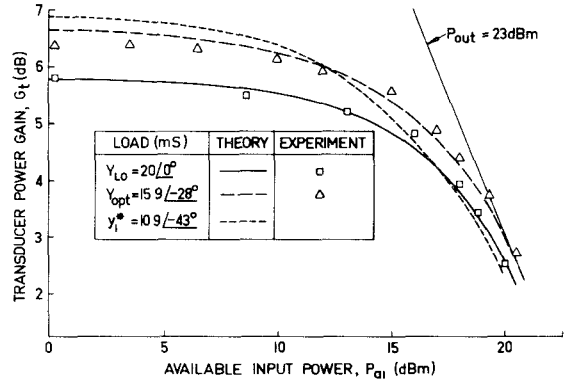


Fig. 4. Transducer power gain $G_t$ against available input power $P_{a1}$ for three different loads. The diagonal line represents a constant output power of $P_{out}=23$ dBm.

The above method for determining the optimum load from measured $S_{22}$ data is most accurate when the $S_{22}$ measurements are carried out at reasonably large power levels. If the power level $P_{a2}$ is too low, then the variation of $G_{out}$ from its small-signal value will be small and may be swamped by measurement errors. For this reason, it is desirable that $P_{a2}$ be greater than the nominal output power of the transistor. In the present example, $P_{a2}$ is 5 dB greater than the 23-dBm nominal output power.

### B. Gain Compression

To calculate gain compression characteristics of the device it is necessary first to determine values for the device parameters $\delta$ and $\beta$. The parameter $\delta$ is obtained from (8). Using a measured value of $G_{pm}=9.38$ dB, (8) yields $\delta=4.32\times 10^{-5}$ $S^3\cdot W^{-1}$. In [9], $\beta$ was determined from measured intermodulation distortion data. In the present work, $\beta$ is obtained from the measured small-signal $s_{21}$ and the large-signal $S_{21}$ at a power level of $P_{a1}=20$ dBm. With these data in (9), one obtains $k=k_s=0.69/5.5°$. Using the relationship

$$P_{in}=P_{a1}\left(1-|S_{11}|^2\right) \tag{26}$$

and substituting the above value for $k$ in (3) with $Y_L=Y_0$, the value of $\beta$ is found to be $4.41/168°$ $W^{-1}$.

Using these values of $\delta$ and $\beta$, the transducer power gain $G_t=P_{out}/P_{a1}$ has been computed as a function of the available input power $P_{a1}$. The calculated $G_t$ is shown in Fig. 4 for three different loads. The first load is the characteristic admittance $Y_0=20$ mS used in the measurement of $S_{21}$. The second load is the calculated $Y_{opt}$ at $P_{opt}=23$ dBm. Experimental data are also shown in Fig. 4. The experimental points for the 20-mS load are taken directly from the $S_{21}$ data in Fig. 1 while the data for the optimum load $Y_{opt}$ were obtained from a separate measurement with 20-mS source admittance and a slug tuner at the output port. Agreement between the experimental data and the theoretical curves is reasonable. The third theoretical gain compression characteristic in Fig. 4 is for a small-signal

conjugate match $y_1^*$ at the output of the transistor. This load produces the maximum gain at low input power levels, but gain compression increases rapidly as the available input power is increased above about 10 dBm.

## VI. Conclusions

The analysis presented here is approximate in nature, but leads to simple expressions for FET large-signal output and forward gain characteristics. It has been shown that at large-signal levels, the optimum FET load admittance $Y_{opt}$ is not simply the complex conjugate of the large-signal output admittance $Y_{out}$. The imaginary parts of these admittances are equal and of opposite sign, but the optimum load conductance is more sensitive to changes in power level than the large-signal output conductance. The large-signal $S$-parameter $S_{22}$, therefore, cannot be used directly as a measure of the optimum load. A method has been given for determining the device output nonlinearity from $S_{22}$ measurements. This technique enables $Y_{opt}$ to be calculated from the relatively easily measured $S_{22}$ and avoids tedious load-pull measurements. Measured $S_{21}$ data can be used to determine the transconductance or forward gain nonlinearity. With these data, the gain-compression characteristics of the transistor can be calculated for any load admittance.

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# A Large-Signal Model for the GaAs MESFET

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***Abstract*— An analytic large-signal model for the GaAs FET is described which relates the terminal currents to the instantaneous terminal voltages and their time derivatives. It incorporates the device geometry and semiconductor parameters as well as the device parasitic circuit elements. The model is fast and efficient when implemented on a computer and is in a form suitable for large-signal circuit design and optimization.**

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## I. Introduction

INCREASINGLY, field-effect transistors (FET's) are finding use in large-signal applications such as microwave power amplifiers [1], [2], oscillators [3], mixers [4], multipliers [5], and pulsed circuits [6]. The principles of FET operation are reasonably well understood, small-signal devices have been modeled [7], and linear circuits have

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